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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/621,292	07/17/2003	Min-Chul San	8021-160 (SS-18118-US)	2476
22150	7590	04/03/2007	EXAMINER	
F. CHAU & ASSOCIATES, LLC 130 WOODBURY ROAD WOODBURY, NY 11797			PHAM, THANH V	
			ART UNIT	PAPER NUMBER
			2823	
SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE		
3 MONTHS	04/03/2007	PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/621,292	SAN ET AL.	
	Examiner	Art Unit	
	Thanh V. Pham	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 27 February 2007.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1,2,5-8,12,13,16-19,22,23 and 26-31 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-2, 5-8, 12-13, 16-19, 22-23, 26-31 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Response to Amendment

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
2. Claims 1, 5-6 and 12, 16-17 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doan et al. US 5,196,360 in combination with Takeuchi US 5,766,997 and Maex et al. US Pub. 2002/0151170 A1.

Re claims 1, 12 and 31, Doan et al. reference discloses a method for fabricating a semiconductor device, figs 1-4, comprising:

forming a field region on a substrate 12 to define an active region; forming a gate pattern 22/14 on the active region, wherein the gate pattern includes sidewalls; forming spacers 24 on the sidewalls of the gate pattern; forming source/drain regions 16/18 aligned with the spacers on both sides of the gate pattern;

forming a metal film (claim 1) of *titanium* layer 28 for silicide on the entire surface of the substrate;

forming a N-rich titanium nitride layer 30 on the *titanium* layer, col. 4, lines 42-54; thermally treating the *titanium* layer 28 for silicide and the N-rich titanium layer 30 to form a *titanium* silicide layer on the gate pattern and the source/ drain region, col. 4, line 55 to col. 5, line 8;

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and selectively removing the *titanium* layer for silicide and the N-rich titanium nitride layer, wherein a top portion of the *titanium* silicide on the gate pattern and the source/drain region is exposed, col. 5, lines 17-21.

The Doan et al. reference does not use Ni-based metal layer comprised of a nickel alloy for silicide on the silicon substrate but uses a metal film. The Doan et al. reference also does not disclose cleaning the substrate using a wet cleaning process.

The Takeuchi reference discloses a method for fabricating a semiconductor device, embodiment 4, comprising:

forming a field region on a substrate 121 to define an active region, fig. 12A;

forming a gate pattern 125 on the active region, wherein the gate pattern includes sidewalls, fig. 12B;

forming spacers 130/131 on the sidewalls of the gate pattern, fig. 12D;

forming source/drain regions 127/128, 132/133 aligned with the spacers on both sides of the gate pattern; “the source region is damaged by ion implantation. Before the silicide layer is formed, therefore, dilute HF cleaning is generally performed to exposed the surface of the silicon substrate”, col. 9, lines 35-37;

forming nickel or titanium or cobalt interchangeably, col. 1's lines 29-30, for a metal layer 136 for silicide on the entire surface of the substrate, or a nickel alloy

a metal which can form silicide when reacted with silicon (this metal will be hereinafter called “silicide forming metal”). This silicide forming metal is, for example, refractory metal, more specifically, at least one kind of metal selected from a group of tungsten (W), cobalt (Co), titanium (Ti) and nickel (Ni). The first metal can be formed by a known thin film forming technology, such as sputtering or CVD, col. 7's lines 30-37.

forming a titanium nitride layer 137 on the Ni-based metal layer 136;

Then, a reaction suppressing layer is formed on the first metal layer including at least above the drain region and excluding above the source region. ...

The reaction suppressing layer is formed of a material which causes no silicidation with silicon, or low-resistance material which may cause a silicidation but has a lower reactivity than the mentioned metal. One example of the material for the reaction suppressing layer is a metal nitride. This metal nitride may be a nitride of the aforementioned silicide forming metal. More specifically, the metal nitride is at least one kind selected from a group of titanium nitride, cobalt nitride, nickel nitride and tungsten nitride. When the reaction suppressing layer is formed of a metal nitride, this metal nitride should not necessarily be a nitride of the same metal as is used for the first metal layer. When a metal nitride is the material for the reaction suppressing layer, this layer may be formed by CVD, sputtering and the other applicable to this process, col. 7, lines 42-62.

thermally treating the Ni-based metal layer comprised of nickel alloy for silicide and the titanium nitride layer to form a nickel silicide layer on the gate pattern and the source/drain region, col. 17, lines 24-30; and

selectively removing the Ni-based metal layer for silicide and the titanium nitride layer, wherein a top portion of the nickel silicide on the gate pattern and the source/drain region is exposed, col. 17, lines 39-41.

The Takeuchi reference does not use N-rich titanium nitride but uses titanium nitride and makes the titanium nitride layer enriched with nitrogen while annealing "under the nitrogen or ammonia environment", col. 8, lines 12-13.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the metal layer for silicide of the Doan et al. reference with material of nickel or nickel alloy as taught by Takeuchi because the nickel layer for silicide of Takeuchi would provide the metal layer for silicide of Doan et al. the same characteristic as analyzed by Takeuchi to enhance the reduction in sheet resistance (Takeuchi's col. 1, lines 24 and 65).

Alternatively, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of Takeuchi with N-rich titanium nitride of Doan because the N-rich titanium nitride of Doan would provide the titanium nitride of Takeuchi with inhibition ability of "outgrowth of silicide and potential short circuit paths between adjacent silicide contact areas" (Doan's abstract).

The combination of Doan et al. and Takeuchi teaches substantially all of the instant steps of fabricating a semiconductor device. The combination does not disclose Ta, Zr, Hf, Pt, Pd, V, Nb or any combination of these (excluding Ti, Co and W).

The Maex et al. reference discloses these materials as elements in a Ni alloy used to formed Ni silicide [0014] or [0019], e.g. Especially [0014] discloses

The first layer structure can also include a cobalt-nickel alloy with the nickel content varying from 0 to 100%; ... Also, other metals such as Pt or Pd can be chosen as elements that are present in the first layer structure.... or the elements Pt and Pd can be added in minor amounts to the first layer structure. Also, other elements such as Au, Ir, Os, Rh, Ti, Ta, W, Mo, Cr, C, and Ge can be part of the first layer structure.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of the combination with Maex et al.'s Ni alloy containing one of Ta, Zr, Hf, Pt, Pd, V, Nb or any combination of these materials because the Ni alloy of Maex et al. would provide the combination with materials that "can withstand thermal treatment without significant degradation" [0009].

In this combination, choice of ratio of elements in the Ni-based metal layer would have been a matter of routine optimization because elements ratio is known to affect device properties and would depend on the desired device density on the finished wafer and the desired device characteristics. One of ordinary skill in the art would have been

led to the recited greater than zero to 20 % of the chosen elements in the alloy through routine experimentation to achieve desired characteristics as suggested by Maex et al.

Further, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide the process of Doan et al. with the step of cleaning the substrate using a wet cleaning process as taught by Takeuchi as the cleaning step would be selected in order to expose the surface of the silicon substrate.

Use of Ni-based metal *comprised of nickel alloy and N-rich titanium nitride* in the combination would provide "the nickel silicide on the gate pattern neither shorted nor cut, a pit is prevented from being formed in a boundary area between the active region and the field region, and lumping of the nickel silicide is prevented and a silicide residue is prevented from remaining on the spacers and the field region" as claimed and well-suited with Doan et al.'s col. 6, line 62 to col. 7, line 6 "for inhibiting outgrowth of adjacent silicide contact areas which have the potential for forming short circuit paths between the silicide contact area" and preventing "pitting of the silicon substrate", Doan et al.'s col. 4, lines 64-68.

Re claims 5 and 16, the Doan et al. reference discloses the chemical formula TiN_x where $x > 1$ or from about 1 to 2 or 1.1 to 1.3 (col. 2, line 8, col. 3, lines 24-31, col. 6, line 8).

Re claims 6 and 17, the Takeuchi reference discloses the thermal treatment for forming nickel silicide layer is carried out using a RTN, col. 8, line 11, not in vacuum but obviously must be in a thermal system.

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3. Claims 2, 7-8 and 13, 18-**19**, 22-**23** and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Doan et al. with Takeuchi and Maex et al. as applied to claims 1, 5-6 and 12, 16-17 and 27-30 above, and further in view of Catabay et al. US 6,503,840 B2, Jaiswal et al. US 6,664,166 B1 and Hill et al. US 6,775,046 B2.

The combination of Doan et al./Takeuchi/Maex et al. teaches substantially all of the instant steps of the method for fabricating a semiconductor device. Although Doan et al. teaches the transistor structure is formed using conventional technique, metal layer 28 for silicide and nitrogen-rich titanium nitride layer 30 are formed by sputtering (col. 4, lines 2-4 and 35-54), and Takeuchi teaches cleaning the surface of the substrate and forming the Ni-based metal layer comprised of nickel alloy and titanium nitride layer by sputtering; none of the reference teaches at what temperature the Ni-based metal layer is formed and using RF sputtering etching to remove particles from the surface of the substrate in situ with the formation of Ni-based layer and TiN layer.

Re claims 2, 13, 19, 22-**23** and 26, the Hill et al. reference teaches

As known, the temperature at which the target is maintained influences the composition of the alloy that is deposited on the substrate during sputtering. As example, if the block of metal in dish 27 is a titanium nickel alloy of 50% titanium and 50% nickel, and that target is at room temperature during the sputtering process, the alloy deposited on the substrate will be different in composition, namely, 48% titanium and 52% nickel. If the target is at 100 degrees C. during the sputtering process, then the composition of the deposited alloy will be 49% titanium and 51% nickel. And if the target is maintained at a temperature of 200 degrees C. during the sputtering process, the deposited alloy will be 50% titanium and 50% nickel, col. 9, lines 34-45.

Choice of temperature in the formation of elements would have been a matter of routine optimization because temperature is known to affect process steps and resulting

device properties and would depend on the desired device density on the finished wafer and the desired device characteristics as taught by Hill et al. One of ordinary skill in the art would have been led to the recited temperature through routine experimentation to achieve desired deposition and reaction rates. It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the process of the combination with the Ni-based metal *comprised of nickel alloy* sputtering with selected temperature of about 25 to 500 °C in a thermal treatment system because the sputtering of Ni-based metal within the selected temperature range in the system would give the process of the combination with the desired metal as taught by Hill et al.

Re claims 7-8, 18-19, 22-23 and 26, the Catabay et al. reference discloses the process wherein the contaminated surface is solvent cleaned to remove residues and then RF cleaned before titanium and then titanium nitride are deposited over the surface in the same chamber, abstract. And/or the Jaiswal et al. reference discloses "a method for processing a partially fabricated semiconductor wafer ... including performing a wet pre-metallization cleaning step on the surface of the wafer, performing an RF plasma sputter etching process ... while maintaining unbroken vacuum conditions ... and depositing a layer of metal on the surface of the wafer ... a stabilization bake cycle then is performed on the wafer", col. 2, lines 50-66.

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the cleaning and depositing of the combination of Doan et al. and Takeuchi with the teachings of Catabay et al. and/or Jaiswal et al. because the steps of cleaning/etching and depositing of Catabay et al. and/or Jaiswal et al. would provide the

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process of Doan et al and Takeuchi with continuous process and preventing further contamination.

Response to Arguments

4. Applicant's arguments filed 02/27/2007 have been fully considered but they are not persuasive.

5. First arguments is the Ni-based metal layer of Takeuchi is not the alloy, the use of alloys would be immediately envisaged by disclosure of "at least one of ..." because of the limited number of species of types of metal 'mixtures'. Further, the "combination thereof" of the provided materials in the claims also does not disclose "additional steps" being "required for turning a mixture/(combination) of metals into an alloy" in the same manner as in Takeuchi.

6. Second argument is based on the canceled cobalt in the claims such that the Maex reference material is "different alloys" than nickel alloy, all include cobalt. Applicant is directed to the quote in the rejection wherein the Maex reference discloses "first layer structure can also include a cobalt-nickel alloy with the nickel content varying from 0 to 100%" and "other elements such as Au, Ir, Os, Rh, Ti, Ta, W, Mo, Cr, C, and Ge can be part of the first layer structure". These extracts mean that with 100% nickel, the material is not all cobalt as alleged; with less than 100% nickel and the added material of one of Ta, Pd, Pt, e.g., the combination satisfies the requirement of all claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-1866. The examiner can normally be reached on M-Th (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

WF

03/27/2007


George Fourson
Primary Examiner